ABSTRACT

A system and method of managing processor instructions provides enhanced performance. The system and method provide for decoding a first instruction into a plurality of operations with a decoder. A first copy of the operations is passed from the decoder to a build engine associated with a trace cache. The system and method further provide for passing a second copy of the operation from the decoder directly to a back end allocation module such that the operations bypass the build engine and the allocation module is in a decoder reading state.